

 <div data-bbox="491 98 536 264"> I Q R </div>	IBIS QUALITY REPORT	date	1 (8)
		23-May-14	

IBIS Quality Report

Company:	STMicroelectronics
IBIS file name	m24c08_fb1_mlp2x3.ibs
IBIS Version:	4.0

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1. MODELING

IBIS (I/O, Buffer, Information, Specification) provide a standardized way, officially EIA standard 656-A-1999 and IEC 62014-1, to model behaviorally a digital component input, output and I/O buffers.

1.1 Component description

Component reference	Technology	Component description
M24C08-W M24C08-R M24C08-F	CMOS F8H/P4	The M24C08 is a 8-Kbit I ² C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 1 K × 8 bits. The M24C08-W can be accessed (Read and Write) with a supply voltage from 2.5V to 5.5V, the M24C08-R can be accessed with a supply voltage from 1.8V to 5.5V, and the M24C08-F can be accessed with a supply voltage from 1.7V to 5.5V

1.2 Modeling conditions

Simulator used	AMS 2010.1 (Mentor Graphics)
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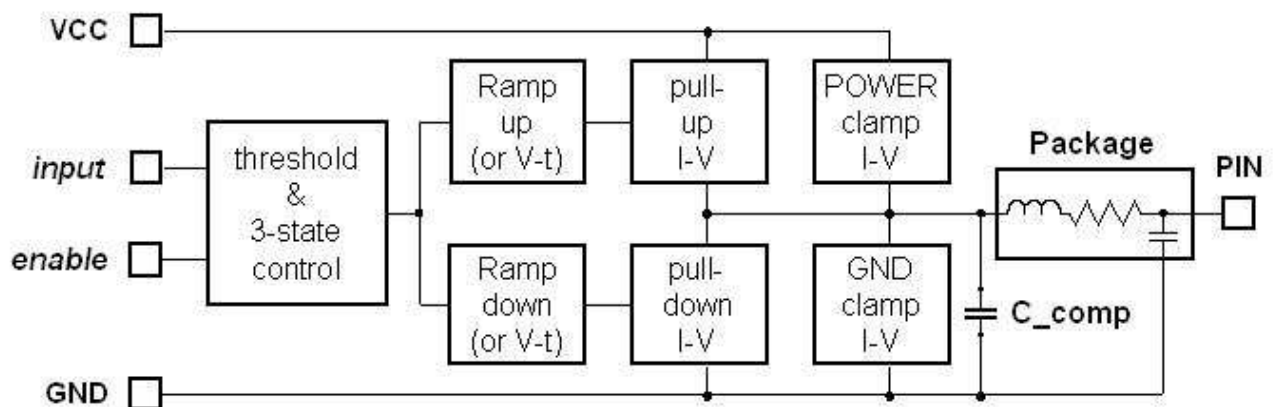


Figure 1 – IBIS model generic structure

conditions	Typical	Minimum	Maximum
Temperature [C°]	25	-40	85
Voltage Supply * [Volt]	1.8	1.7	2.0
Process setting	nom	weak	strong

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* Different Voltage Reference (only if Voltage Supply is not present)	Typical	Minimum	Maximum
Pullup Voltage Reference [Volt]	-	-	-
Pulldown Voltage Reference [Volt]	-	-	-
Power Clamp Voltage Reference [Volt]	-	-	-
GND Clamp Voltage Reference [Volt]	-	-	-

Model names (of Component)	Model Type	C_comp (typ, min, max)
mod_sda	I/O_Open_Drain	2.024pF (typ), 1.845pF(min) , 2.119pF (max)
mod_scl	Input	1.763pF (typ), 1.683pF (min) , 1.933pF (max)
mod_wc	Input	1.763pF (typ), 1.683pF (min) , 1.933pF (max)

Model names (of Component)	Threshold and Vmeas	Timing parameters (if used)
mod_scl/wc	Vinl=0.54V , Vih=1.26V	
mod_sda	Vmeas=9.00V	Rref=1k, Cref=10pF, Vref=1.80V

Package	description/comment
MLP 2x3	8 lead micro leadframe outline

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1.3 Circuit for data extraction

The I-V data are extracted by simulations using the simulation setup shown in figure 2 below. This model is an I/O model, other model type derived from this structure. For more accurate modeling, certain combinations of V-T tables are recommended (with exception of Input-only model types) using the simulation setup shown in figure 3, with load conditions specified.

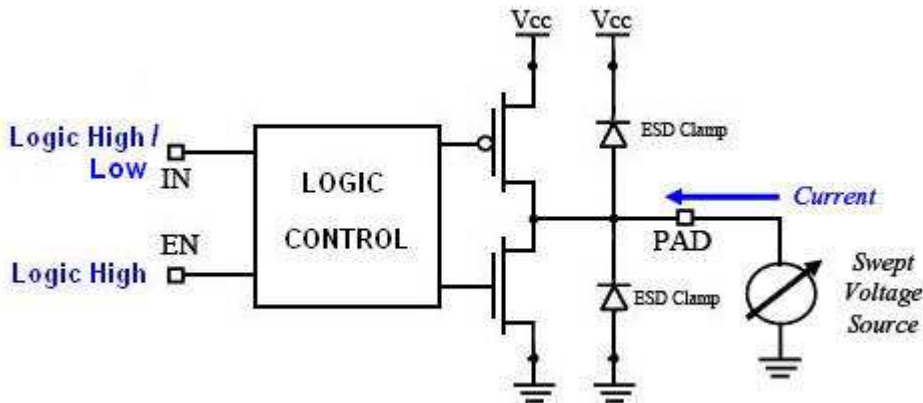


Figure 2 – Simulation Setup to extract I/V data from I/O model type

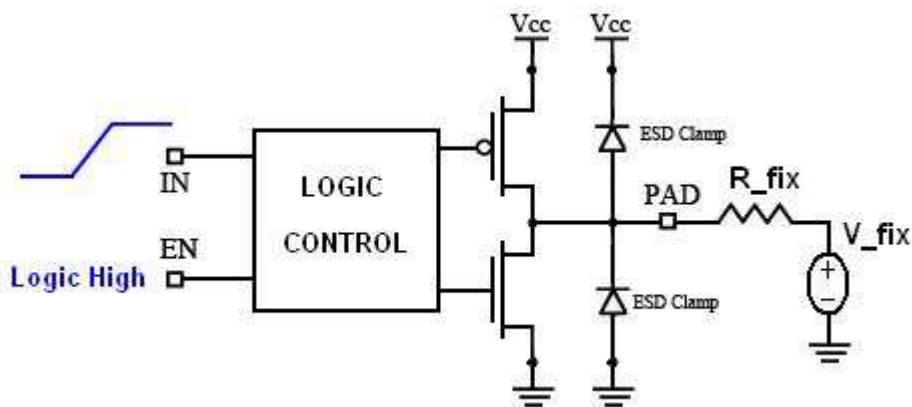


Figure 3 – Simulation Setup to extract V/T data from I/O model type

Extracting V/T conditions:

V-T data condition extractions	Load conditions	Adding conditions
Rising waveform	R_fix=50 Ohm, V_fix= 0 V	
Rising waveform	R_fix=50 Ohm, V_fix= 1.8 V	
Falling waveform	R_fix=50 Ohm, V_fix= 1.8 V	
Falling waveform	R_fix=50 Ohm, V_fix= 0 V	

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2. IBISCHK5 CHECK

The created IBIS model must be checked using IBISCHK5 parser to ensure that the syntax is correct. The result of the check is showed in the next section with some comments (optional).

2.1 Result Check by IBISCHK5

IBISCHK5 V5.0.4

Checking m24c08_fb1_mlp2x3.ibs for IBIS 4.2 Compatibility...

NOTE (line 94) - Pulldown Typical data is non-monotonic

NOTE (line 94) - Pulldown Minimum data is non-monotonic

NOTE (line 94) - Pulldown Maximum data is non-monotonic

WARNING - Combined Pulldown for Model: mod_sda Typical data is non-monotonic

WARNING - Combined Pulldown for Model: mod_sda Minimum data is non-monotonic

WARNING - Combined Pulldown for Model: mod_sda Maximum data is non-monotonic

Errors : 0

Warnings: 3

File Passed

Adding comments about the Warning or Note:
<p>The output check contains some Note about non-monotonic data of I-V curves, but they are not indicative of problems inside the model.</p>

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3. FUNCTIONAL CHECK

The created IBIS model must be compared with the Original Buffer circuit. The signal outputs, in the same load conditions (figure 4), must be mached. These output comparisons are presented in TYP, MIN and MAX condition. This section can't be defined for Input and Terminator model type, because they are input-only model types.

How well results are matched?	Put "X" into the right filed
Curves shape match correctly, but there is a little time translation.	
Curves shape match correctly, but there is a mismatch into the Overshot and/or Undershot regions.	
Curves match well.	X

3.1 Functional verification:

Circuit used for output comparison results is illustrated in figure 4.

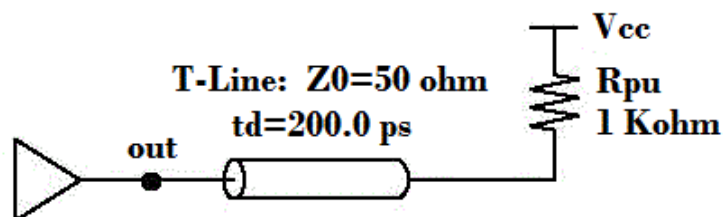


Figure 4 – Circuit used for Functional Check

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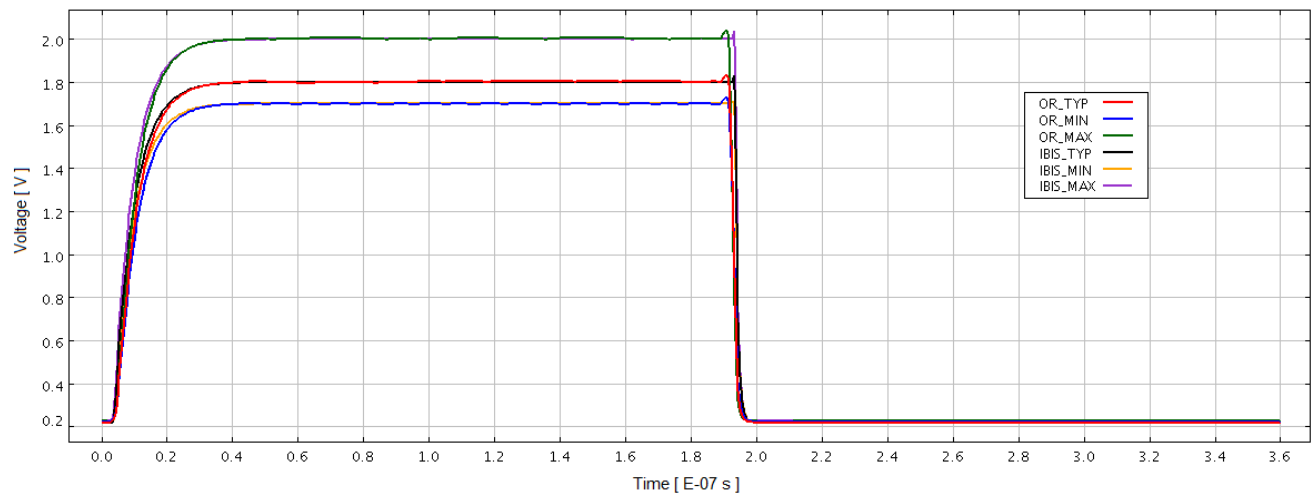


Figure 5 – IBIS vs Eldo comparison results of “mod_sda” Model

Output Comparisons:

Adding comments about the comparison:

4. EXTRA INFORMATION

This section can contains other extra informations, to explain some other features of peculiar IBIS model

Other specifications	description